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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,502	11/15/2003	Clair John Glossner III	YOR919990548US4 (8728-341	9966

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F. CHAU & ASSOCIATES, LLP
1900 Hempstead Turnpike, Suite 501
East Meadow, NY 11554

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,502	GLOSSNER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,12,13,19,23,24,30,34-53,55,56 and 58-60.* is/are rejected.

7)☒ Claim(s) *3-7,9-11,14-18,20-22,25-29,31-33,54 and 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-60 are presented for examination.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 2,13,24 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 19, 29,39 of prior U.S. Patent No. 6,665,790. This is a double patenting rejection.

As to claims 2,13,24, claims 2,13,24 are dependent claims from claims 1,12,23, respectively. Claims 2,13,24 include all the limitations in the respective parent claims 1,12,23. Considering all limitations, claims 2,13,24 are the same as patented claims 19,29, 39.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1(58),12(59),23(60) are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 19,29, 39 , respectively, of U.S. Patent No. 6,665,790. Although the conflicting claims are not identical, they are not patentably distinct from each other because while the current claims 1,12,23 do not have the additional feature of the storage element identified by any given entry includes the arbitrary starting address in the vector data file for any entry in the pointer array as recited in the patented claims 19,29,39, it would have been obvious to one of ordinary skill in the art to omit the identification by any entry in the pointer array for the patented claims 19, 29,39 already taught the identification of the storage element by a particular entry and by any entry in the pointer array (e.g. see patented claim 19, lines 7-11, lines 12-14), therefore, omission of identifying the storage element by any entry would have eliminated the overhead of identifying the non-particular storage data element entry, and therefore,, reducing the overall time constraints of the storage of the given data elements, and in doing , provided a motivation.

3. As to claims 58,59,60, clams 58,59,60 are the same as claims 1,12,23. This might have been overlooked by applicant. Examiner believes that this is a minor error due to clerical error. Applicant is kindly suggested to provide correction in next response. For purpose of examination, claims 58,59,60 have been treaded (see page 9 below).

4. Claim 34 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,665,790. Although the conflicting claims are not identical, they are not patentably distinct from each other because while current claim 34 does not include the specific features of the identifying and accessing the vector portions as claimed, it would have been obvious to one of ordinary skill in the art to omit the identification and access of the vector portions based on the teaching already taught in patented claim 1 which taught the performance of the specified operation (lines 15-17) , which would have been recognizable by one of ordinary skill in the art that any specific format of specifying the operations would not change the main scope of the invention, that is the operation performance on the arbitrary vector portions would not be affected. For the above reasons, claim 34 is found obvious over the patented claim 1.

5. Claims 34-42,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5,669,013) in view Karp et al. (5,689,653).

As to claims 34, 43, Watanabe disclosed a vector processing system (e.g. see figs. 1-5) comprising at least :

a) loading a vector (e.g. see the loading in col.5, lines 44-61, col.6, lines 15-18, lines 45-47, col.7, lines 20-22, col.11, lines 11, lines 5-9);

b)accessing portions of a vector (see the access of the vector elements in col.5 lines 2-32, see also the vector elements in the matrix example in col.13, lines 10-58, see also figs.4 for configuration of the vector);

c)performing a specified operations using accessed vector portions (e.g. see col.5, lines 2-32, see specific operation in col.13, lines 10-58).

6. Watanabe did not specifically show to access of the vector portions was "arbitrary" as claimed. However, Karp disclosed a vector system including arbitrarily vector length (e.g. see the vector identifying information specified by instruction col.4, lines 61-66, see the identifying information, vector length and the arbitrary size in col.5, lines 13-32, it arbitrary because it was designated by instruction). It would have been obvious to one of ordinary skill in the art to use Karp in Watanabe for accessing arbitrary vector portions as claimed because the use of Karp could enhance the processing capability of vector registers in Watanabe for providing a greater number of vector elements at a given request , thereby expanding the processing structure of Watanabe, and it could be readily achieved by configuring the arbitrary vector portions of Karp into Watanabe, such that the specific number of vector elements could be accessed, and because Watanabe also disclosed that his vector data was being transferred between one group of vector registers and the processing unit in the

foreground, while vector data was being transferred between another group of vector registers and the main memory to make available vector data and that pointers were used for keeping track of the order of array elements (e.g. see col.1, lines 60-67, col.2, lines 1-5, col.2, lines 19-21), which was a suggestion of the need of an arbitrary set of vector portions (e.g. in the foreground and background) in order to reduce the wait time of processing unit, and in doing so, provided a motivation. Watanabe is used as primary reference because it showed clearly the loading of vector, the access of vector portions, and the performance of the specified operation (see operation example in col.13, lines 10-58). Karp is used as secondary because it showed clearly the particular teaching of the arbitrary portions (see the vector length designated by instruction in col.5, line 13-32, col.4, lines 61-66).

7. As to claims 35-37, Watanabe also included :

a)obtain pointer information (e.g. see figs. 4A-F, fig.5 [302], col.5, lines 7-13);

b)identifying the portions of vector using pointer information (e.g. see col.5, lines 7-13, col.9, lines 45-67, col.10, lines 1-6);

c) accessing identified portion of vector (e.g. see .col.5, lines 7-13, col.9, lines 45-67, col.10, lines 1-6);

d)updating the pointer information (e.g. see the advance of the pointer in col.9, lines 53-56, col.10, lines 50-55).

8. As to claim 38, Karp was also directed to non-sequential read because it included discontinuous vector data elements (see col.11, lines 16-30).

9. As to claims 39,40, Watanabe also included indirect read and write (see the mapped vector addresses in col.5, lines 57-67).

10. As to claim 41, Karp also included stride value (e.g. see col.5, lines 12-14).

11. As to claim 42, Watanabe also included modulo addressing access (see the modulor counter for the vector in col.10, lines 46-49).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 44 –51,55,56 are rejected under 35 U.S.C. 102(a) (b) as being anticipated by Karp et al. (5,689,653).

13. As to claim 44, Karp taught loading of vector boundary [address of starting vector element] for accessing portions of a vector [vector] (see col.5, lines 15-18).

14. As to claims 45, 46, the word "arbitrary" is read as information can be designated by instruction or program. Karp also included arbitrary addresses (see the address value was specified by instruction in col.4, lines 61-66).

15. As to claim 47, Karp also included a load instruction (see the memory load in col.1, lines 48-52).

16. As to claim 48, Karp taught :

a) a vector memory area (see vector in memory 46 in col.4, lines 32-33) ;

b) controller for performing operation (transfer operation) on arbitrary portions (starting address, vector length) of a vector stored in the memory area (see the vector identifying information specified by instruction col.4, lines 61-66, see the identifying information : vector length and the arbitrary size in col.5, lines 13-32, it arbitrary because it was designated by the instruction).

17. As to claim 49, Karp also included a pointer [address value] (see col.5, lines 13-18).

18. As to claim 50, Karp also included a pointer memory area (see the 64 bit long address pointer in col.5, lines 13-18).

19. As to claim 51, Karp also included a load instruction (see the memory load in col.1, lines 48-52).

20. As to claims 55, as to the "rows" and "columns", since no specific format of the rows and columns is being recited, it is read as a general type of a memory format. Karp's memory 46 should have the row and column structure based on the RAM memory already taght in col.3, lines 26-33.

21. As to claim 56, Karp also taught linear array because the address value to access the memory was a 64-bit value (col.5, lines 13-18), which represented 2 to the 64 possible address values.

22. Claim 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp (5,689,653) in view of Pawate et al. (5,528,550).

23. As to claims 52,53, limitations of the parent claims 49,48 have been discussed in paragraph # 16,17. Karp did not specifically show the memory area including a plurality of pointers or the pointer array as claimed. However, Pawate disclosed a pointer array including a plurality of pointers (See the last element of each vector V pointing to the next vector Vn-1 in fig.4, col. 5, lines 65-67, col.6, lines 1-3). It would have been obvious to one of ordinary skill in the art to use Pawate in Karp for including the pointer array as claimed because the use of Pawate could provide Karp the efficient control of the vector data in a predetermined set of the vector access sequence, thereby increasing the efficiency of the vector access in a given group of vector search., and because Karp also disclosed a plurality of registers for transferring the vectors (e.g. see col.6, lines 15-25) , which was an indication of a need for using a memory array for storing a plurality of pointer values in order to reduce the hardware latency on the address registers, and in doing so, provided a motivation.

24. Claim 1,8,12,19,23,30, 58,59 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5,669,013) In view of Karp et al (5,689,653) in view of Pawate et al. (5,528,550) .

25. As to claims 1, 8,58, Watanabe taught :

a)a vector data file comprising a plurality of storage elements for storing data elements of the data vectors (e.g. see the vector registers in figs. 4A-F, col.5, lines 1-61);

b) pointer identifying the vector elements in the data file (e.g. figs.4 A-F, see col.5, lines 1-61);

c)a starting address in the vector file (e.g. see col.5, lines 1-12).

26. As to claim 8, each entry of the pointer array (linked list) of Pawate also included a starting address of at least one storage element (e.g. see the last field of each vector V pointing to the starting address of the next vector Vn-1 in fig.4,, col.5, lines 65-67, col.6, lines 1-3).

27. Watanabe did not specifically show to access of the vector portions was "arbitrary" as claimed. However, Karp disclosed a vector system including arbitrarily vector length (e.g. see the vector identifying information specified by instruction col.4, lines 61-66, see the identifying information, vector length and the arbitrary size in col.5, lines 13-32, it arbitrary because it was designated by instruction). It would have been obvious to one of ordinary skill in the art to use Karp in Watanabe for accessing arbitrary vector portions as claimed because the use of Karp could enhance the processing capability of vector registers in Watanabe for providing a greater number of vector elements at a given request , thereby expanding the processing structure of Watanabe, and it could be readily achieved by configuring the arbitrary vector portions of Karp into Watanabe, such that the specific number of vector elements could be accessed, and because Watanabe also disclosed that his vector data was being transferred between one group of vector registers and the processing unit in the

foreground, while vector data was being transferred between another group of vector registers and the main memory to make available vector data and that pointers were used for keeping track of the order of array elements (e.g. see col.1, lines 60-67, col.2, lines 1-5, col.2, lines 19-21), which was a suggestion of the need of an arbitrary set of vector portions (e.g. in the foreground and background) in order to reduce the wait time of processing unit, and in doing so, provided a motivation.

28. Neither Watanabe nor Karp specifically show the pointer array as claimed. However, Pawate disclosed a vector processing system including a pointer array including a plurality of pointers (See the link list of the pointers in fig.4, col. 5, lines 65-67, col.6, lines 1-3). It would have been obvious to one of ordinary skill in the art to use Pawate in Watanabe for including the pointers array as claimed because the use of Pawate could provide Watanabe the efficient control of the vector data in a predetermined set of the vector access sequence, thereby increasing the efficiency of the vector access in a given vector search request., and because Watanabe also disclosed more complex vector access system, such as the submatrices implementations (see the matrix applications in Appendices), and pointers were used in tracking the order of vector elements (col.2, lines 19-21), which would have required the use of a pointer array to adapt to complex variables in the matrix expressions, and in doing so, provided a motivation.

29. As to claims 12,19, 23,30, 59,60 , each entry of the pointer array (linked list) of Pawate also included a starting address of at least one storage element (e.g. see the last field of each vector V pointing to the starting address of the next vector Vn-1 in fig.4,, col.5, lines 65-67, col.6, lines 1-3).

30. Watanabe taught :

a) providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors (e.g. see the vector registers in figs. 4A-F, col.5, lines 1-61);

b) providing a pointer identifying the vector elements in the data file (e.g. figs.4 A-F, see col.5, lines 1-61);

c) providing a starting address in the vector file (e.g. see col.5, lines 1-12).

31. Watanabe did not specifically show his starting address was an arbitrary starting address as claimed. However Karp disclosed a vector system including arbitrarily vector length (e.g. see the vector identifying information specified by instruction col.4, lines 61-66, see the identifying information, vector length and the arbitrary size in col.5, lines 13-32, it arbitrary because it was designated by instruction). It would have been obvious to use Karp in Watanabe as claimed. The reasons have been given in Paragraph # 27 above, therefore, it will not be repeated herein.

32. Neither Watanabe not Karp specifically showed the pointer array as claimed. However, Pawate disclosed a vector processing system including a pointer array

including a plurality of pointers (See the link list of the pointers in fig.4, col. 5, lines 65-67, col.6, lines 1-3). It would have been obvious to one of ordinary skill in the art to use Pawate in Watanabe for including the pointers array as claimed for the reasons already given in the Paragraph # 28 above, there it will not be repeated herein.

33. Claims 3-7, 14-18,25-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the entry in the pointer array which was updated based on the data read out from an entry I the vector data file.

34. Claims 9,10, 20,21,31,32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the matrix of rows and columns represented by an entry in the pointer array.

35. Claims 11,22,,33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the feature of the storage element identified by any entry was independent with respect to at least one storage element identified by other entries of the pointer array for any given entry in the pointer array.

36. Claims 54 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the pointer array includes the address representing the row and column of element in the vector memory.

37. Claim 57 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the pointer array organized in a matrix of rows and columns.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP